REMARKS

Claims 1-14 currently remain in the application. Claims 1, 2, 6-8, 12 and 13 have been amended.

Double Patenting

Claims 1-12 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-12 of U.S. patent No. 6, 488, 581. A terminal disclaimer is included with this amendment and the rejection is believed overcome thereby.

Rejections under 35 U.S.C. § 112

Claims 2, 6, 8 and 12-14 are rejected under 35 U.S.C. § 112, second paragraph. Claims 2, 6, 8 and 12 have been amended for the purposes of clarification to remove the "at least partially" term objected to by the Examiner and the rejection is believed overcome thereby.

Claim 13 has been amended to depend from claim 12 and the rejection to claims 13 and 14 are believed overcome thereby.

Rejections under 35 U.S.C. § 103

The Examiner rejected claims 1, 3 and 5 under U.S.C. 103 (a) as being unpatentable over Sugai (5,564,036) in view of Ciciora (US patent No. 4,091, 418). The rejection is respectfully traversed.

The claims describe, as recited in claim 1, for instance, a mass storage device command latch for storing commands from a disk controller; a timing circuit for timing signals between the mass storage device command latch and the mass storage device; a comparator between the mass storage device command latch and the timing circuit; and a comparator command register in communication with the comparator, the comparator command register including ATA write commands where the comparator issues a fault when the mass storage device command latch stores a command matching an ATA command from the comparator command register.

Prior IDE systems known to the Applicant were designed to allow read and write operations to a mass storage device. The IDE standard provides as much; it defines a set of read and write commands. There was no incentive to prevent writing to an IDE mass storage device. It is only in the context of a gaming machine where one confronts a need to disable the write capabilities of the IDE protocol in a manner that a fault is issued when a write is detected. The claims recite a system that protects a mass storage device or an IDE mass storage device in a gaming machine from write operations. To this effect, the claims require that the comparator command register include ATA write commands that can be compared against commands from a disk controller. The comparator issues a fault when the mass storage device command latch stores a command matching an ATA command from the comparator command register. Typically, the fault will cause the gaming machine to cease gaming operations which is a feature unique to gaming.

Sugai, Cols. 1 and 2, describes detecting addresses in RAM and writing those addresses into latch memory by the CPU. Because Sugai does not protect mass storage devices but RAM from write operations, does not detect commands, only addresses, where the addresses are provided by the CPU not the disk controller, it is respectfully submitted that pending claims are patentable over the Sugai patent. Ciciora does not overcome these deficiencies. All claims require a system that can detect ATA write commands where the comparator issues a fault when the mass storage device command latch stores a command matching an ATA command from the comparator command register where the mass storage device command latch stores commands from a disk controller. These limitations are not taught or suggested by Sugai or Ciciora. Therefore, for at least these reasons, Sugai and Ciciora alone or in combination can't be said to render obvious the present invention and the rejection of claims 1, 3 and 5 is believed overcome thereby.

The Examiner rejected claims 2, 4 and 6 under U.S.C. 103 (a) as being unpatentable over Sugai (5,564,036) in view of Ciciora (4,091, 418) and in further view of Browne (6,272,533). The rejection is respectfully traversed.

Examiner has stated in the office action that Sugai and Ciciora lack disclosing a control and status register in communication with the comparator command register and the comparator. The invention as recited in claims 2, 4 and 6 requires "a control and status register in communication with the comparator command register and the comparator wherein the control and status register is configured to receive information from the comparator and to send information to the comparator command register and is operable to receive information from a jumper for enabling writing to the mass storage device." Browne does not describe a comparator, a comparator command register or a jumper and how they are connected. Further, details of the circuits used in Browne are not provided. Thus, Browne can't be said to overcome the deficiencies recited in regards to Sugai and Ciciora by the Examiner. Therefore, for at least these reason, the combination Sugai, Ciciora and Browne can't be said to render obvious claim 2, 4 and 6 and the rejection is believed overcome thereby.

The Examiner rejected claims 7, 9 and 11 under U.S.C. 103 (a) as being unpatentable over Sugai (5,564,036) in view of Ciciora (4,091, 418) and in further view of Brunner, et al. (4,727,544). The rejection is respectfully traversed.

The Sugai and Ciciora patents have been distinguished above. The Brunner patent describes a method of software computation of a checksum to ensure the integrity of data stored in EPROMs. Brunner also specifies a method of software computation to ensure that the data stored in these local memories is valid. It does not disclose or suggest a system for protecting its EPROM from write operations.

In gaming machines, as described by Brunner, the EPROM are protected from writes because, by design, EPROMs do not allow writes. Thus, the gaming machine in Brunner does

not provide any mechanisms for writing to an EPROM. This differs from differs from the RAM of Sugai that is normally written to in the course of operating the device in Sugai. On gaming machines, such as those described in Brunner, game programs are updated by physically replacing the EPROM with a new EPROM. The system of Brunner is for confirming that an authorized EPROM has not been installed in the gaming machine not for protecting the EPROM from writes. Thus, because Brunner does not overcome the deficiencies described in regards to Sugai and Ciciora and because Brunner does not teach or suggest a system for protecting memory from writes, the combination of Sugai, Ciciora and Brunner can't be said to render obvious claims 7, 9 and 11 and the rejection is believed overcome thereby.

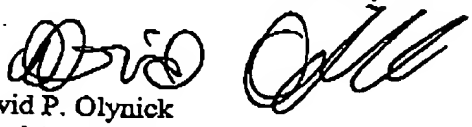
The Examiner rejected claims 8, 10 and 12-14 under U.S.C. 103 (a) as being unpatentable over Sugai (5,564,036) in view of Ciciora (4,091, 418) and in further view of Brunner, et al. (4,727,544) in further view of Browne (6,272,533). The rejection is respectfully traversed.

As described above, the combination Sugai, Ciciora and Browne does not provided, as recite, "a control and status register in communication with the comparator command register and the comparator wherein the control and status register is configured to receive information from the comparator and to be accessible to the comparator command register and is operable to receive information from a jumper for enabling writing to the mass storage device." A control and status register is not taught or suggest in Sugai and Ciciora. Browne or Brunner does not describe a control and status register configured to receive information from the comparator and to send information to the comparator command register and operable to receive information from a jumper for enabling writing to the mass storage device. Therefore, for at least these reasons, the combination of Sugai, Ciciora, Browne and Brunner can't be said to render obvious claims 8, 10 and 12-14 and the rejection is believed overcome thereby.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a

telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



David P. Olynick
Reg. No.: 48,615

P.O. Box 778
Berkeley, CA 94704-0778
510-843-6200